Comparative Study and Mathematical Modeling of Power Dissipation in 6-Transistor SRAM and 7-Transistor SRAM

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***Abstract*- In this paper, we have proposed the concept of 7-Transistor SRAM. 7-Transistor SRAM has been designed to provide an interface with CPU and to replace DRAM in systems that require very low power consumption. The feature of 7-Transistor SRAM like low power consumption and leakage current have been analyzed with 45nm technology. The comparative study and mathematical modeling have been proposed for 6-Transistor SRAM and 7-Transistor SRAM with the help of various performance parameters like Aspect Ratio, Area and Delay Considerations.**

Keywords- SRAM, 6-Transistor SRAM, 7-Transistor SRAM and Leakage Current.

I. INTRODUCTION

SRAMs are used in various devices like laptops and several electronic gadgets. With the scaling technology the threshold voltage is also decreasing due to which there is a significant increase in the leakage current. Since SRAMs have high speed and low power consumption so they are largely used in cache memories[1].

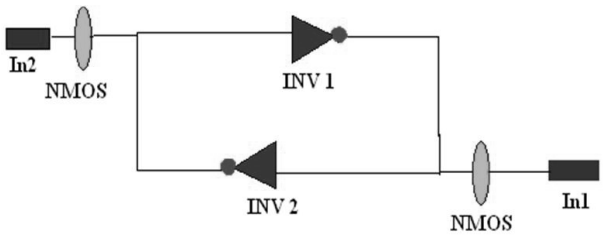

Fig.1:Basic SRAM Cell

SRAM (static random access memory) falls in the category of volatile semi conductor memories. It has been used to store binary logics '1' and '0'. SRAM consists of bi-stable latch circuitry in which two inverters has been used for storing each binary bit. Simplest SRAM cell consists of two inveters which are cross coupled as mentioned in fig.1.Two complementary lines are connected via inverters for communicating with the outside world[2].

SRAMs are easy to use and they have low leakage current, therefore they are widely used in mobile applications. The demand for low power devices has been increased in recent years due to the fast growth of battery operated applications such as PDAs, cell phones, laptops etc. Cache occupy more than 50% of chip area and leakage power dissipation is proportional to area. To reduce the power consumption low supply voltage is used and thus we get low leakage SRAM circuits [12]. Several types of leakage currents occurring in SRAM cells are subthreshold, gate leakage current, leakage current minor amount of GIBL and DIBL [14].

CMOS technology have become so advanced that it has become possible to design the circuits of high integration density, small size and low power consumption**.** All the above features can be achieved with the help of scaling technology. But the drawback of technology-scaling is that there has been a tremendous increase in leakage current. This along with the power dissipation has become the major problem of VLSI industries. Several measures have been taken to mitigate the effects of leakage current problem and power dissipation such as decrease in supply voltage, increase in threshold voltage etc. In this paper, we have proposed the concept of 7-Transistor SRAM because in 6-Transistor SRAM faced the problem of stability at very small feature sizes. In 7-Transistor SRAM pre-charging and balancing scheme has been introduced which saved 45% of power as compared to 6-

Transistor SRAM cell. But there is a tradeoff between area and power consumption in 7 transistor SRAM cell[3].

II. Classification of SRAM

A.By Transistor

Bipolar junction transistor (used in TTL and ECL) has a very high speed but consumes lots of power and MOSFET (used in CMOS) consumes less power but most frequently used [9].

B. By Function

1. Asynchronous: Operation doesn't depend upon the clock frequency. Datain and data out are controlled by address transition.

2. Synchronous: As the demand of fast SRAM necessitated, there is a variation done in asynchronous SRAM. Its operation depends upon the clock frequency thus read and write cycles synchronization is done with the microprocessor clock so it can be used in very high speed applications. Cache SRAM memory is the main application of synchronous SRAM. Here address, datain and all control signals are associated with the clock signals[9].

III. Architecture Of 1 Bit SRAM Cell

For write operation, write enable="1". For Read and Write operations word enable should be kept high. In SRAM, Read and Write operations cannot be performed simultaneously as shown in fig.2.

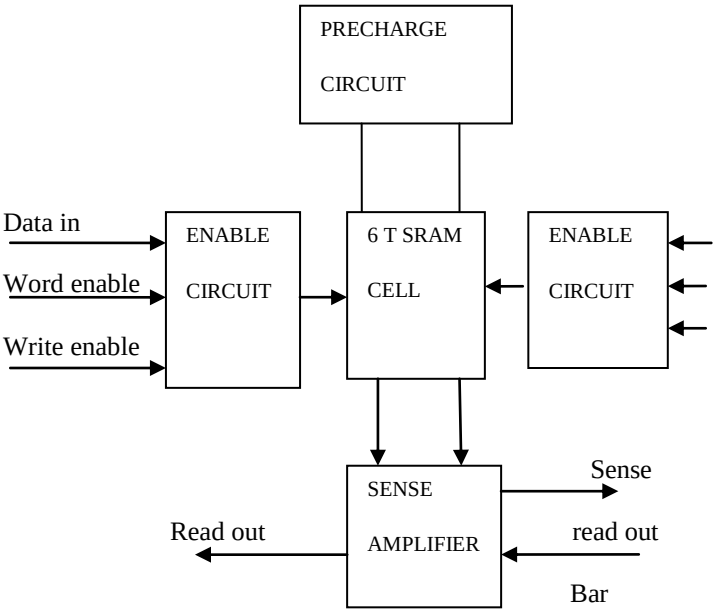

Fig.2: Architecture of 1 Bit Basic SRAM Cell

A.Precharge

The bit and bit bar lines has been charged to 5V with the help of Precharge circuit. During read and write operations bit is kept low as shown in fig.3.

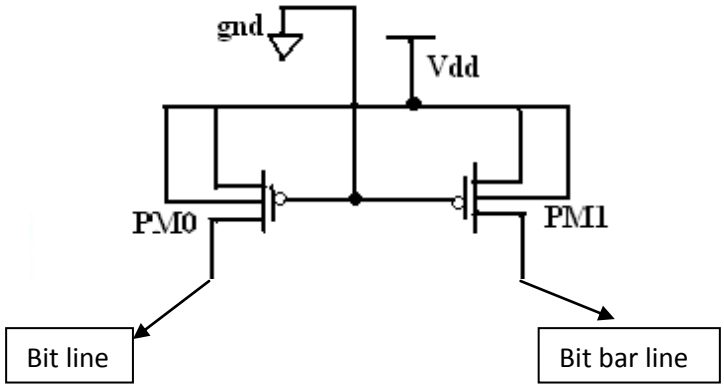

Fig.3: Precharge Circuit

PM0, PM1 are PMOS transistors and their gates have been grounded. Due to grounding of PMOS gates they will be turned ON and thus bit and bit bar lines goes to Vdd level.

B.Data Enable Circuit

For turning PM6 and NM3 ON write enable should be high. This makes a way into bit or bit bar line for data. Thus, write operation is performed when write enable="1" as shown in fig.4.

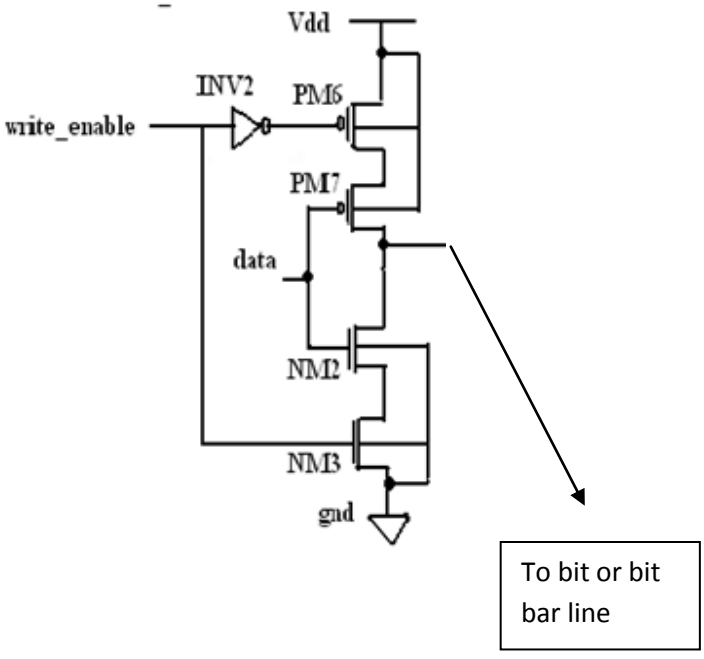

Fig.4: Data Enable Circuit

C .Sense Amplifier

For reading the data sense amplifier is used. It also reduces delay and minimizes the power consumption of whole chip. Low voltage sense amplifier is used for high performance.

IV. 6 Transistor SRAM

In a 6 transistor SRAM when a bit is stored, it functions as a latch. The total leakage power consumption in SRAM cell is given by the sum of leakage current of both the inverters. As we have been using cross coupled inverters, the area consumed is high which is considered as a drawback[4]. Data storage nodes are being accessed by pass transistors which are connected to the bit lines. Voltage division is the cause of disturbance of storage nodes as shown in fig.5[1].

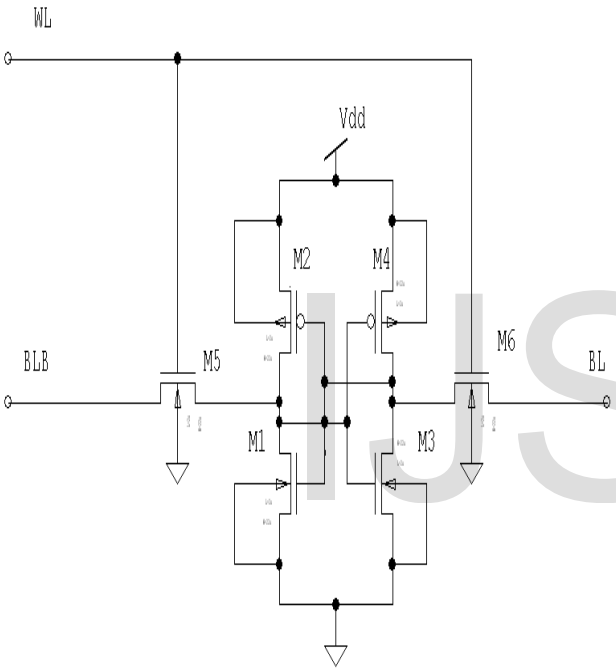

Fig.5: 6 transistor SRAM Cell

V. 7 Transistor SRAM

Due to high power consumption in 6 transistor SRAM a low overhead read/write circuitry has been proposed in 7 transistor SRAM with an additional transistor as shown in fig.6 which includes two PMOS and five NMOS transistors. Pass transistors have been used here and they are connected to both the bit lines. RWL and WWL have been used for reading and writing operations respectively.

The power consumed in write operation has been reduced by 31% and speed has been enhanced by 31%. Read power is decreased by 60% and total average power consumption has been reduced by 45%[4]. Due to the isolation of storage nodes from the bit lines, during the read operation, the data stability is significantly improved as compared to 6 transistor SRAM.

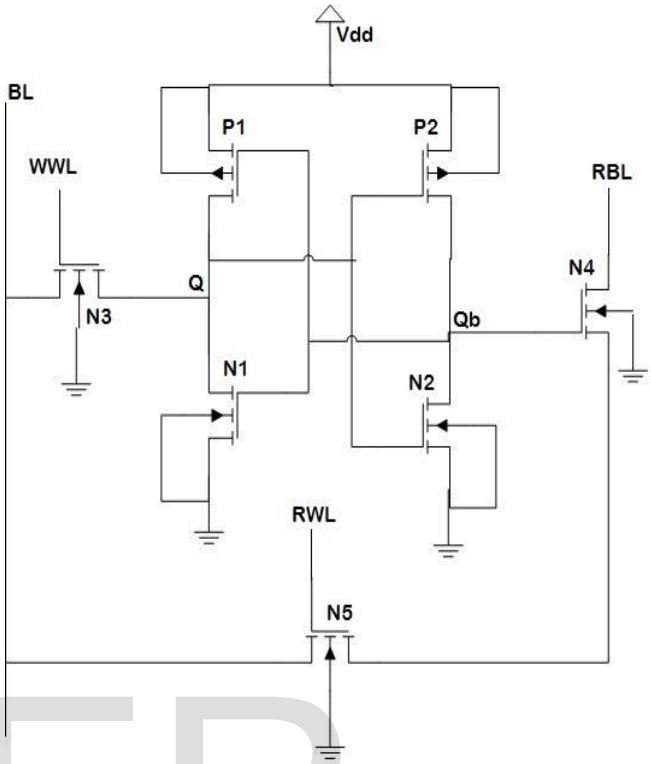

Fig.6: 7 Transistor SRAM Cell

VI. Mathematical Modeling of 6 Transistor SRAM

A. Data Hold State

For "WL=0", M1 and M2 disconnects the cell from bit lines. Since the transistors are in off state therefore leakage current will flow.

B.Data Read State

Initially precharging bit and bit bar are kept high. With reference to fig.5. M3 and M6 are turned on WL="1" which turns ON the M1 and M2. Thus the outputs of both the inverters are transferred to bit lines through M5 and M6. Since M2 is OFF thus M2 and M6 pull bit bar HIGH. Consequently bit line discharges through M1 and M3.

C.Data Write State

WL="1" and the value that we have to write is applied to the bit lines. Thus, if data "0" is to be written, we assert Bit="0", Bit bar="1" and to write data "1", the Bit ="1",Bit bar="0"[4].

D.Standby Mode

The transistors M5 and M6 disconnect the cell from the bitline if the word line is not pronounced. From the two cross coupled inverters the transistors M1 and M4 continues to strengthen each other until power supply is ON[8].

VII. Mathematical Modeling of 7 Transistor SRAM

With reference to the fig.6 leakage current and dynamic power consumption is reduced due to the charge transfer from read to write bit line. No additional precharge circuitry is required here for write operation instead of this a write driver will pull the bit line high or low depending on input data. Read word line (RWL) and write word line (WWL) have been used to control read and write operations respectively[6].

A.Read Operation

Firstly, RBL is precharged to Vdd. During the read phase RWL is maintained at logic high and WWL is at logic low. If Qb="1" then RBL is discharged through N4 and N5 to bitline and if Qb="0" RBL is maintained at logic high. Read bit line RBL and write bit line WBL shares the charge during the read operation consequently the storage points Q and Qb gets completely isolated from bitline[6].

B.Write Operation

Here BL is already at mid level voltage and the write driver has to pull it from mid level to full swing voltage. During the write phase WWL is maintained at logic high while RWL is at logic low. The data is written to Q through access transistor N3.The transistor stack formation between N4 and N5 reduces the leakage current[6].

C.Hold Operation

During hold operation Q and Qb stores the data, until the power supply is available, due to its volatile nature. If Qb="1" and Q="0" then stored data is "0" and alternatively if Q="1" and Qb="0" then stored data is "1"[7].

VIII. Comparative Study between 6 transistor and 7 transistor SRAM

Table 1: Comparison Between 6T and 7T SRAM

PARAMETERS	6T SRAM	7T SRAM
Area	less	more
Leakage Current	high	less
Power Consumption	high	less
Word Line	one	two

The power consumed in write operation has been reduced by 31% and speed has been enhanced by 31%. Read power is decreased by 60% and total average power consumption has been reduced by 45%[4].

IX. Conclusion

In this paper, the feedback connection between the two back to back connected inverters is being cut down with the help of a proposed write methodology. Though this technique uses an extra transistor but it helps in reducing power consumption upto a great extent. The simulation has been carried out using cadence tool and much better tolerance is achieved using 7 Transistor SRAM cell[10]. It is very necessary to maintain the balance between read and write operations. Instead of focusing on sizing of transistors, redesigning of bit structure should be given the priority[5]. The structure obtained although is more stable but there is a tradeoff between area and asymmetric configuration. It is more suitable for the devices which are to be kept in static mode for larger duration of time[4].

X. Future Scope

GBI's research states that in 2020 there will be wide market available for SRAM's. Low power consumption and large bandwidth make these devices more suitable in electronic appliances such as digital cameras, cell phones etc. There are several companies working on SRAM technology such as Cypress Semiconductor, Samsung Semiconductor, Micron Technology, Inc., Integrated Device Technology, Inc.,Integrated Silicon Solution, Inc., GSI Technology[13]. This paper can be extended to work on area reduction which is more as compared to existing SRAM cell. SRAM is used in cache memories in processors as well as in embedded systems. Due to advancement in IC technology, SRAM's are widely used in embedded system. The SRAM cells is becoming indispensable block in SOC's[11].

XI. Acknowledgement

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